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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,371	03/19/2004	James E. Miller JR.	2269-7550.6US (96-0570.06)	7223
24247 . 7590	06/20/2007		EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			TU, CHRISTINE TRINH LE	
			ART UNIT	PAPER NUMBER
			2117	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/804,371

Applicant(s)

MILLER, JAMES E.

Examiner

Christine T. Tu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 37-39 and 55-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 37-39 and 55-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>March 19, 2004</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. Claims 1-36 and 40-54 have been cancelled.
2. Claims 37-39 (Group I) have been elected without traverse (as stated on page 5 in the remarks of Applicant's response filed on May 18, 2007).
3. Claims 55-64 have been added.
4. Claims 37-39 and 55-64 have been examined.

Claim Objections

5. Claim 55 is objected to because of the following informalities:

As per claim 55, at line 2, the phrase "o f" should be replaced with the word "of".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claims 60-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 60:

It is not clear how a latch mode, an input signal, an output signal are interrelated to the test mode blocking signals.

The steps throughout the claim are not coherent; the steps appear not to be interrelated to each other. Therefore, it is not clear how these steps carry out the step of "initiating a test mode blocking signal".

Claims 61-64:

These claims are rejected because they depend on claim 60 and contain the same problems of indefiniteness.

7. The following rejections are based on the best understanding of the claimed invention by the examiner in view of the ambiguities that exist in the claims as mentioned above (¶ 6).

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 37-39 and 55-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sprouse et al. (5,951,703 and Sprouse hereinafter).

Claims 37, 39 and 58-59:

Sprouse teaches the invention substantially as claimed. Sprouse discloses (figure 1) a digital system (10) having a control logic unit (20) for controlling individual digital subsystems (12a, 12b, ..., 12n). The scan logic (20) supplies the hold, scan and bypass signals as test signals to selectively place the subsystems (12) in either a normal mode or scan mode. When the control logic (20) asserts the scan signal to initiate the scan test mode, the elemental memory states (30) of each subsystem are reconfigured to a formation of scan strings via the scan data lines (sdi_1, \dots, sdi_n) and scanned out via the scan data out lines (sdo_1, \dots, sdo_n). (figures 1-3, column 3 line 65-column 4 line 49, and columns 5-6).

Sprouse does not explicitly teach the initiating a test mode block signal. Sprouse, however, teaches that the scan control logic (20) asserts a scan signal to initiate the scan test mode (column 5 lines 26-36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Sprouse' scan control logic (20) would have also assert a hold signal or a bypass signal to initiate the normal mode. One having ordinary skill in the art would be motivated to realize so because Sprouse teaches that normal (non-test) operation is formed when scan control logic (20) asserts the hold signal, or both bypass and scan signals (column 6 lines 39-46, column 6 lines 18-24).

Claims 38 and 56:

Sprouse teaches the scan data outputs (sdo_1, \dots, sdo_n) are sent back to the scan control logic unit (20) for analysis (column 8 lines 39-45).

Claim 55:

Sprouse teaches the receiving of the system enable (sys_enable) from the multiplexer (52) (figure 3, column 6 lines 5-8).

Claim 57:

Sprouse does not explicitly teach the gating of test mode entry function with one of an OR, NOR, AND and NAND logic gate. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that

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Sprouse' hold signal or Sprouse' bypass signal would have been gated by one of an OR, NOR, AND and NAND logic gate. One having ordinary skill in the art would be motivated to realize so because there is no particular purpose being recited for gating the test mode entry function in the limitation of this claim,

Claim 60:

Sprouse' subsystems (20) accepts the scan data inputs (sdi_1, \dots, sdi_n), Sprouse' memory stages (30) within each of the subsystems (20) perform logic operations on the inputs, each subsystem (20) provides a scan data output (Sdo) (figures 1-3).

Sprouse does not explicitly teach the initiating a test mode block signal. Sprouse, however, teaches that the scan control logic (20) asserts a scan signal to initiate the scan test mode (column 5 lines 26-36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Sprouse' scan control logic (20) would have also assert a hold signal or a bypass signal to initiate the normal mode. One having ordinary skill in the art would be motivated to realize so because Sprouse teaches that normal (non-test) operation is formed when scan control logic (20) asserts the hold signal, or both bypass and scan signals (column 6 lines 39-46, column 6 lines 18-24).

Claim 61:

Each of Sprouse' subsystems (20) provides a scan data output (Sdo_1, \dots, Sdo_n) and then sends back to the scan control logic unit (20) (figure 1).

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Claims 62-64:

Sprouse teaches the receiving of the system enable (sys_enable) from the multiplexer (52) (figure 3, column 6 lines 5-8).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571) 272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Christine T. Tu
Primary Examiner
Art Unit 2117

June 16, 2007